WHAT IS CLAIMED is:

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1. A semiconductor device having active regions connected together by interconnect layers comprising:

first and second transistors formed spaced apart from each other in a semiconductor substrate, each of the first and second transistors having active regions;

an isolation region formed between the first and second transistors in the semiconductor substrate for isolating the first and second transistors from each other;

at least one slit formed in the surface of the isolation region to allow those paired active regions of the first and second transistors which are opposed to each other with the isolation region interposed therebetween to communicate with each other through it, the slit having inner walls and a predetermined width;

a conductive layer formed on the inner walls of the slit; and

an interconnect layer having first and second portions respectively formed on the paired active regions of the first and second transistors so that each of them is electrically connected with a corresponding one of the paired active regions, and a third portion formed along the slit on the isolation region, the first, second and third portions being made integral with one another.

2. The device according to claim 1, wherein

the at least one slit consists of one slit.

3. The device according to claim 1, wherein the at least one slit consists of a plurality of slits parallel with one another.

4. The device according to claim 1, wherein the slit has a minimum value of its width set to the minimum dimension determined by processing accuracy and a maximum value set such that the slit can be substantially filled up with the third portion of the interconnect layer.

5. The device according to claim 4, wherein the minimum value of the slit width is 0.03 μm and the maximum value is 0.1 μm.

6. The device according to claim 1, wherein a depth of the slit is less than that of the isolation region.

7. The device according to claim 1, wherein the conductive layer is a silicon-containing film.

8. The device according to claim 7, wherein the silicon-containing film is a polysilicon film.

9. The device according to claim 1, wherein the interconnect layer has a stacked structure including a lower layer of silicon and an upper layer of metal silicide.

10. The device according to claim 1, wherein the interconnect layer has a stacked structure including a lower layer of an alloy of silicon and germanium and

an upper layer of silicide of an alloy of silicon and germanium.

11. The device according to claim 1, further comprising a contact portion formed on the third portion of the interconnect layer.

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12. A semiconductor device having active regions connected together by an interconnect layer comprising:

first and second MOS transistors formed spaced apart from each other in a semiconductor substrate, each of the first and second MOS transistors having a gate electrode and active regions;

an isolation region formed between the first and second MOS transistors in the semiconductor substrate for isolating the first and second MOS transistors from each other;

at least one slit formed in the surface of the isolation region to allow paired active regions of the first and second MOS transistors, which are opposed to each other with the isolation region interposed therebetween, to communicate with each other through it, the slit having inner walls and a predetermined width;

a conductive layer formed on the inner walls of the slit;

a gate electrode of another MOS transistor formed above the isolation region; and

an interconnect layer having first and second

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portions respectively formed on the paired active regions of the first and second MOS transistors so that each of them is electrically connected with a corresponding one of the paired active regions, and a third portion formed along the slit on the isolation region to ride on and be electrically connected with the gate electrode of another transistor, the first, second and third portions being made integral with one another.

13. The device according to claim 12, wherein the at least one slit consists of one slit.

14. The device according to claim 12, wherein the at least one slit consists of a plurality of slits parallel with one another.

15. The device according to claim 12, wherein the slit has a minimum value of its width set to the minimum dimension determined by processing accuracy and a maximum value set such that the slit can be substantially filled up with the third portion of the interconnect layer.

16. The device according to claim 15, wherein the minimum value of the slit width is 0.03 μm and the maximum value is 0.1 μm.

17. The device according to claim 12, wherein a depth of the slit is less than that of the isolation region.

18. The device according to claim 12, wherein

the conductive film is a silicon-containing film.

19. The device according to claim 18, wherein the silicon-containing film is a polysilicon film.

20. The device according to claim 12, wherein the interconnect layer has a stacked structure including a lower layer of silicon and an upper layer of metal silicide.

21. The device according to claim 12, wherein the interconnect layer has a stacked structure including a lower layer of an alloy of silicon and germanium and an upper layer of silicide of an alloy of silicon and germanium.

22. The device according to claim 12, further comprising a contact portion formed on the third portion of the interconnect layer.

23. A method of manufacturing a semiconductor device having active regions connected together by an interconnect layer comprising:

forming first and second device regions in a semiconductor substrate so that they are isolated from each other by an isolation region formed in the semiconductor substrate;

forming at least one slit in the surface of the isolation region so that the first and second device regions communicate with each other through it, the slit having inner walls and a predetermined width;

depositing a conductive layer, which includes

a material that can form a nucleus for epitaxial growth, over the entire surface of the semiconductor substrate and then selectively removing the conductive layer so that it is left on the surface of a portion of each of the first and second device regions and on the inner walls of the slit; and

covering the periphery of the conductive film left on the portion of each of the first and second device regions with a material serving as a block for epitaxial growth and then epitaxially growing a conductive film so as to form an interconnect layer having first and second portions respectively located on the first and second device regions and a third portion located on the isolation region to run along the slit, the first, second and third portions being made integral with one another.

24. The method according to claim 23, wherein one slit is formed in the isolation region.

25. The method according to claim 23, wherein a plurality of slits is formed in the isolation region in parallel with one another.

26. The method according to claim 23, wherein the slit has a minimum value of its width set to the minimum dimension determined by processing accuracy and a maximum value set such that the slit can be substantially filled up with the third portion of the interconnect layer.

27. The method according to claim 26, wherein the minimum value of the slit width is 0.03 μm and the maximum value is 0.1 μm.

28. The method according to claim 23, wherein the slit is formed so that its bottom does not reach the bottom of the isolation region.

29. The method according to claim 23, wherein the conductive film includes a silicon-containing film.

30. The method according to claim 29, wherein the silicon-containing film is a polysilicon film.

31. The method according to claim 23, wherein the interconnect layer is formed to have a stacked structure including a lower layer of silicon and an upper layer of metal silicide.

32. The method according to claim 23, wherein the interconnect layer is formed to have a stacked structure including a lower layer of an alloy of silicon and germanium and an upper layer of silicon-germanium alloy silicide.

33. The method according to claim 23, further comprising forming a contact portion on the third portion of the interconnect layer.

34. A method of manufacturing a semiconductor device having active regions connected together by an interconnect layer comprising:

forming first and second device regions in the surface of a semiconductor substrate so that they are

isolated from each other by an isolation region formed in the semiconductor substrate;

forming at least one slit in the surface of the isolation region so that the first and second device regions communicate with each other through it, the slit having inner walls and a predetermined width;

depositing a conductive film, which includes a material that can form a nucleus for epitaxial growth, over the entire surface of the semiconductor substrate and then selectively removing the conductive film so that it is left on the surface of a portion of each of the first and second device regions and the isolation region and the inner walls of the slit;

covering the periphery of the conductive film left on the portion of each of the first and second device regions and the isolation region with a material serving as a block for epitaxial growth;

selectively removing, of the block forming material covering the conductive material left on the portion of the isolation region, its portion which is located in the vicinity of the slit; and

epitaxially growing a conductive film so as to form an interconnect layer having first and second portions respectively located on the first and second device regions and a third portion located on the isolation region to run along the slit and ride on the conductive film on the portion of the isolation region

having the block forming material removed, the first, second and third portions being made integral with one another.

35. The method according to claim 34, wherein one slit is formed in the isolation region.

36. The method according to claim 34, wherein a plurality of slits is formed in the isolation region in parallel with one another.

37. The method according to claim 34, wherein the slit has a minimum value of its width set to the minimum dimension determined by processing accuracy and a maximum value set such that the slit can be substantially filled up with the third portion of the interconnect layer.

38. The method according to claim 37, wherein the minimum value of the slit width is 0.03 μm and the maximum value is 0.1 μm.

39. The method according to claim 34, wherein the slit is formed so that its bottom does not reach the bottom of the isolation region.

40. The method according to claim 34, wherein the conductive film is a silicon-containing film.

41. The method according to claim 40, wherein the silicon-containing film is a polysilicon film.

42. The method according to claim 34, wherein the interconnect layer is formed to have a stacked structure including a lower layer of silicon and

an upper layer of metal silicide.

43. The method according to claim 34, wherein the interconnect layer is formed to have a stacked structure including a lower layer of an alloy of silicon and germanium and an upper layer of silicon-germanium alloy silicide.

44. The method according to claim 34, further comprising forming a contact portion on the third portion of the interconnect layer.